

**In the Claims**

1-37. (Canceled)

38. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying region of a substrate layer, comprising:

- a substrate layer having a first substrate region and a second substrate region;
- an oxide region overlying at least a portion of the second substrate region, wherein the oxide region includes a highest upper surface distal the substrate layer;
- a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than the highest upper surface of the oxide region, wherein the lowest upper surface of the first polycrystalline silicon layer is distal the substrate layer; and
- a second polycrystalline silicon layer overlying the first substrate region.

39. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

- a substrate layer having a first substrate region and a second substrate region;
- an oxide region overlying at least a portion of the second substrate region, wherein the oxide region includes a highest upper surface distal the substrate layer;
- a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than the highest upper surface of the oxide region;
- an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and
- a second polycrystalline silicon layer overlying the etch stop layer and the first substrate region.

40. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region, the oxide region including an upper surface distal the substrate layer and a lower surface proximal the substrate layer, the upper surface including a highest upper surface portion of the upper surface of the oxide region, the highest upper surface portion being a most distal portion of the upper surface relative to the substrate layer;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region, the first polycrystalline silicon layer including an upper surface distal the substrate layer and a lower surface proximal the substrate layer, the upper surface of the first polycrystalline silicon layer including a lowest upper surface portion that is a most proximal portion of upper surface of the first polycrystalline silicon layer with respect to the substrate layer and having a thickness selected such that the lowest upper surface of the first polycrystalline silicon layer is higher than the highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the etch stop layer and the first substrate region, the upper surface of the second polycrystalline silicon layer being substantially planar and aligned with the upper surface of the first polycrystalline silicon layer adjacent an interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer such that the interface has no horizontal component.

41. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

a field oxide region overlying at least a portion of the second substrate region;

a gate oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the field oxide and gate oxide regions but not

the first substrate region and having a thickness selected such that the lowest upper surface of the first polycrystalline silicon layer is higher than the highest upper surface of the oxide regions;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer.

42. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

a polycrystalline silicon plug overlying the first substrate region and having the upper surface thereof aligned with an upper surface of the polycrystalline silicon layer adjacent the second substrate region such that a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug has no horizontal component; and

a photoresist mask of material resistant to polycrystalline silicon etching overlying the polycrystalline silicon plug and an adjacent portion of the polycrystalline silicon layer surrounding the polycrystalline silicon plug thereby defining an electrical interconnect.

43. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a polycrystalline silicon layer overlying the oxide region but not the first substrate region

and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

a polycrystalline silicon plug overlying the first substrate region and having an upper surface thereof aligned with an upper surface of the polycrystalline silicon layer adjacent the second substrate region such that a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug has no horizontal component; and

a photoresist mask overlying the polycrystalline silicon plug to define an electrical interconnect.

44. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

at least one oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer.

45. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a polycrystalline silicon plug overlying the first substrate region; and

a polycrystalline silicon layer overlying a portion of the oxide region adjacent the polycrystalline silicon plug, but not the first substrate region, the polycrystalline silicon layer

having a thickness selected such that a lowest upper surface of the polycrystalline silicon layer is higher than a highest upper surface of the oxide region, the polycrystalline silicon layer also having an upper surface thereof in the region adjacent the polycrystalline silicon plug aligned with an upper surface of the polycrystalline silicon plug such that the vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug has no horizontal component.

46. (Canceled)

47. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

- a substrate layer having a first substrate region and a second substrate region;

- at least one oxide region overlying at least a portion of the second substrate region;

- a first polycrystalline silicon layer overlying a portion of the oxide region adjacent the first substrate region, but not the first substrate region, and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

- an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

- a second polycrystalline silicon layer overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer.

48. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

- a substrate layer having a first substrate region and a second substrate region;

- an oxide region overlying at least a portion of the second substrate region;

- a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium layer overlying the etch stop layer and the polycrystalline silicon plug layer.

49. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug;

a titanium layer overlying the etch stop layer; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug layer.

50. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug layer.

51. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a buried contact region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that the lowest upper surface of the first polycrystalline silicon layer is higher than the highest upper surface of the oxide region;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug.

52. (Previously Presented) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer partially overlying the oxide region adjacent the first substrate region but not overlying the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;



a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug.

53. (Previously Presented) The intermediate of claim 38 wherein the first substrate region includes a buried contact region.

54. (Previously Presented) The intermediate of claim 38 wherein a portion of the second polycrystalline layer overlying the first polycrystalline layer is removed to expose the first polycrystalline layer and eliminate a horizontal interface between the first and second polycrystalline silicon layers.

55. (Previously Presented) The intermediate of claim 39 wherein a portion of the second polycrystalline silicon layer overlying the first polycrystalline layer is removed so that a total height of the first polycrystalline silicon layer plus a height of the etch stop layer defines a maximum height of the second polycrystalline silicon layer after removal of the portion of the second polycrystalline silicon layer.

56. (Previously Presented) The intermediate of claim 40 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity.

57. (Previously Presented) The intermediate of claim 56 wherein the first and second polycrystalline silicon layers are doped with arsenic.

58. (Previously Presented) The intermediate of claim 41 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity.



59. (Previously Presented) The intermediate of claim 58 wherein the first and second polycrystalline silicon layers are doped with arsenic.
60. (Previously Presented) The intermediate of claim 42 wherein the polycrystalline silicon plug forms a gate for a field effect transistor.
61. (Previously Presented) The intermediate of claim 43 wherein the polycrystalline silicon plug forms a gate for a field effect transistor.
62. (Previously Presented) The intermediate of claim 44 wherein a photoresist mask is applied over a portion of the first etch stop layer and the second polycrystalline silicon layer.
63. (Previously Presented) The intermediate of claim 62 wherein a titanium layer is deposited to overlie the etch stop layer and the second polycrystalline silicon layer.
64. (Previously Presented) The intermediate of claim 45 wherein the polycrystalline plug and the polycrystalline silicon layer are doped to increase their conductivity.
65. (Previously Presented) The intermediate of claim 64 wherein the polycrystalline plug and the polycrystalline silicon layer are doped with arsenic.
- 66-67. (Canceled)
68. (Previously Presented) The intermediate of claim 47 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity.
69. (Previously Presented) The intermediate of claim 68 wherein the first and second polycrystalline silicon layers are doped with arsenic.

70. (Previously Presented) The intermediate of claim 48 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

71. (Previously Presented) The intermediate of claim 70 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

72. (Previously Presented) The intermediate of claim 49 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

73. (Previously Presented) The intermediate of claim 72 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

74. (Previously Presented) The intermediate of claim 50 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

75. (Previously Presented) The intermediate of claim 74 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

76. (Previously Presented) The intermediate of claim 51 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

77. (Previously Presented) The intermediate of claim 76 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

78. (Previously Presented) The intermediate of claim 52 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

79. (Previously Presented) The intermediate of claim 78 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

80. (Previously Presented) The intermediate of claim 38, wherein the second polycrystalline silicon layer overlies the first polycrystalline silicon layer.

81. (Currently Amended) The intermediate of claim 80, wherein the second polycrystalline silicon layer [[doe]] does not overly the second substrate layer.

82. (Previously Presented) The intermediate of claim 38, wherein the lowest upper surface of the first polycrystalline silicon layer is adjacent the first substrate region.

83. (Previously Presented) The intermediate of claim 38, wherein the second polycrystalline silicon layer is only over the first polycrystalline silicon layer.